IN THE CLAIMS

The claims are not amended, but are presented herein for convenience.

1. (Previously Presented) A communications interface, comprising:

a bus interface coupleable to an internal bus;

a plurality of transmit channels coupled to the bus interface;

a transmit control block coupled to the plurality of transmit channels;

a plurality of outbound links coupled to a plurality of outputs of the transmit control block;

a plurality of receive channels coupled to the bus interface; and

a receive control block coupled to the plurality of receive channels; and

a plurality of inbound links coupled to a plurality of inputs of the receive control block, the inbound links and the outbound links to couple the bus interface to a further bus interface; and

a stop message channel coupled to the receive control block and adapted to send a stop message to a source when a receive FIFO reaches a stop threshold value; and

a start message channel coupled to the receive control block and adapted to send a start message to the source when the receive FIFO reaches a start threshold value.

2. (Original) The communications interface of claim 1, further comprising a direct memory access controller coupled to the bus interface.

3. (Original) The communications interface of claim 1, wherein the bus interface comprises a plurality of transmit control registers and a plurality of receive control registers.

4. (Original) The communications interface of claim 3, wherein the plurality of transmit control registers comprises at least one of:

an interface width register coupled to the transmit control block;

a transmit first in first out (FIFO) register associated with each transmit channel;

an end of message (EOM) register associated with each transmit channel;

an interface interrupt identification register coupled to the transmit control block;

a transmit frequency select register coupled to the transmit control block;

a wait count register coupled to the transmit control block;

a clock stop time register coupled to the transmit control block;

a channel configuration register associated with each transmit channel; and

a channel status register associated with each transmit channel.

5. (Original) The communications interface of claim 3, wherein the plurality of receive control registers comprises at least one of:

a receive FIFO register coupled to each receive channel;

an interface width register to select a predetermined number of bits to be received across the communications interface by the receive control block;

a channel stop register associated with each receive channel;

a channel start register associated with each receive channel;

a wake up register associated with at least one receive channel;

an end of message register associated with each receive channel;

a channel configuration register associated with each receive channel; and

a channel status register associated with each receive channel.

6. (Original) The communications interface of claim 1, wherein each of the plurality of transmit channels and each of the plurality of receive channels comprises a first in first out (FIFO) memory device.

7. (Original) The communications interface of claim 1, further comprising a power management unit coupled to each of the plurality of transmit channels and receive channels.

8. (Original) The communications interface of claim 1, wherein the transmit control block comprises a channel arbiter adapted to select a next one of the plurality of transmit channels to be activated.

9. (Original) The communications interface of claim 1, wherein the transmit control block comprises a link controller adapted to transmit data from a selected transmit channel across a selected link.

10. (Original) The communications interface of claim 1, wherein the receive control block comprises a state machine adapted to store a current active channel number, a number of bits in a current byte being transferred and to write each byte to a selected one of the plurality of receive channels.

11. (Original) The communications interface of claim 1, wherein the plurality of transmit channels comprises:

at least one channel adapted to send a clock signal;

at least one channel adapted to send a strobe signal;

at least one channel adapted to send a wait signal; and

at least one channel adapted to send data.

12. (Original) The communications interface of claim 1, wherein the plurality of receive channels comprises:

at least one channel adapted to send a clock signal;

at least one channel adapted to send a strobe signal;

at least one channel adapted to send a wait signal; and

at least one channel adapted to send data.

13. (Original) The communications interface of claim 1, wherein at least one of the plurality of transmit channels and the plurality of receive channels comprise a virtual general purpose input/output channel.

14. (Previously Presented) The communications interface of claim 1, further comprising:

a channel stop threshold register adapted to set the stop threshold value to cause the stop message to be sent to the source when the receive FIFO is full; and

a channel start threshold register adapted to set the start threshold value to cause the start message to be sent to the source when the receive FIFO can receive additional data.

15. (Canceled)

16. (Original) The communications interface of claim 1, further comprising at least one of a direct flow control mode and a message flow control to control a flow of data across the communications interface.

17. (Original) The communications interface of claim 1, wherein the transmit control block comprises:

a multiplexer coupled to the plurality of transmit channels;

a parallel in serial out converter (PISO) coupled to the multiplexer; and

a control circuit coupled to the multiplexer and the PISO and adapted to select one of the plurality of transmit channels to transmit data.

18. (Original) The communications interface of claim 1, wherein the receive control block comprises:

a demultiplexer coupled to the plurality of receive channels;

a serial in parallel out converter (SIPO); and

a control circuit coupled to the demultiplexer and adapted to select one of the plurality of receive channels to receive data.

19 - 27. (Canceled)

28. (Previously Presented) A method of transmitting data between semiconductor chips, comprising:

writing data into at least one of a plurality of transmit FIFOs;

selecting one of the plurality of transmit FIFOs that contains data to be transmitted and that is not in a wait state; and

transmitting the data to a corresponding one of a plurality of receive FIFOs that has not exceeded a threshold value; and

sending a stop message if the corresponding one of the receive FIFOs cannot receive data; and

sending a start message when the corresponding one of the receive FIFOs can receive data.

29. (Previously Presented) The method of claim 28, further comprising:

sending a wait signal to a transmit control block if the corresponding one of the receive FIFOs cannot receive data; and

removing the wait signal when the corresponding one of the receive FIFOs can receive data; and

sending a stop message if the corresponding one of the receive FIFOs cannot receive data; and

sending a start message when the corresponding one of the receive FIFOs can receive data.

30. (Original) The method of claim 28, further comprising selecting another one of the plurality of transmit FIFOs to send data to another corresponding one of the plurality of receive FIFOs while the corresponding one of the receive FIFOs cannot receive data.

31. (Original) The method of claim 28, further comprising:

sending a strobe signal to initiate a transmission of data;

sending a selected channel number over which the data is to be transmitted; and

sending an end of message signal after the data has been transmitted.

32. (Canceled)

33. (Original) The method of claim 28, further comprising:

selecting one of the plurality of transmit FIFOs and the corresponding one of the plurality of receive FIFOs by a predetermined algorithm.

34. (Original) The method of claim 28, wherein the predetermined algorithm is round-robin.

35. (Original) The method of claim 28, further comprising selecting a interface width from one of a serial width, a two-bit width and a nibble width.

36. (Previously Presented) A method of forming a communications interface, comprising:

forming a bus interface;

forming a plurality of transmit channels coupled to the bus interface;

forming a transmit control block coupled to the plurality of transmit channels;

forming a plurality of outbound links coupled to a plurality of outputs of the transmit control block;

forming a plurality of receive control channels coupled to the bus interface;

forming a receive control block coupled to the plurality of receive control channels; and

forming a plurality of inbound links coupled to a plurality of inputs of the receive control block, the inbound links and the outbound links to couple the bus interface to a further bus interface; and

forming a stop message channel coupled to the receive control block and adapted to send a stop message to a source when a receive FIFO reaches a stop threshold value; and

forming a start message channel coupled to the receive control block and adapted to send a start message to the source when the receive FIFO reaches a start threshold value.

37. (Original) The method of claim 36, wherein forming the bus interface comprises forming a plurality of transmit control registers and a plurality of receive control registers.

38. (Original) The method of claim 36, wherein forming the transmit control block comprises:

forming a channel arbiter adapted to determine a next one of the plurality of channels to be activated; and

forming a link controller adapted to transmit data from a selected transmit channel across a selected link.

39. (Original) The method of claim 36, wherein forming the receive control block comprises forming a state machine adapted to store a currently active channel number, a number of bits in a current byte being transferred and to write each byte to a selected one of the plurality of receive channels.

40. (Original) The method of claim 36, wherein forming the plurality of transmit channels and forming the plurality of receive channels, each comprises:

forming at least one channel adapted to send a clock signal;

forming at least one channel adapted to send a strobe signal;

forming at least one channel adapted to send a wait signal; and

forming at least one channel adapted to send data.

41. (Original) The method of claim 36, further comprising forming at least one virtual general purpose input/output channel.

42. (Original) The method of claim 36, wherein forming the transmit control block comprises:

forming a multiplexer coupled to the plurality of transmit channels;

forming a parallel in serial out converter (PISO) coupled to the multiplexer; and

forming a control circuit coupled to the multiplexer and to the PISO.

43. (Previously Presented) The method of claim 36, wherein forming the receive control block comprises:

forming a demultiplexer coupled to the plurality of receive channels;

forming a serial in parallel out converter (SIPO);

forming a control circuit coupled to the demultiplexer and adapted to select one of the plurality of receive channels to receive data.

44. (Previously Presented) A method, comprising:

supplying a clock signal from a first terminal;

supplying a strobe signal from a second terminal;

providing an identification value corresponding to a selected channel register from data terminals when the strobe signal is active;

providing data from the selected channel register at the data terminals when the strobe signal is inactive, the data changing in accordance with the clock signal; and

providing a third terminal that receives a wait signal that keeps the data provided at the data terminals from changing; and

providing a stop message channel coupled to the receive control block and adapted to send a stop message to a source when a receive FIFO reaches a stop threshold value; and

providing a start message channel coupled to the receive control block and adapted to send a start message to the source when the receive FIFO reaches a start threshold value.

45. - 48. (Canceled)

49. (Previously Presented) The communications interface of claim 1, further comprising:

a channel stop threshold register to store the stop threshold value to cause the stop message to be sent to the source when an amount of data in the receive FIFO exceeds the stop threshold value; and

a channel start threshold register to store the start threshold value to cause the start message to be sent to the source when an amount of data in the receive FIFO falls below the start threshold value.